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Newark and New Brunswick

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Accounting Information Systems

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A.I.S. Class 27: Outline

- Group Work for Chapter 5
- Learning Objectives for Chapter 11
- Information Systems Auditing
- Group Work for Chapter 11
- Hardware Performance
- Group Evaluation Forms

Group Work for Chapter 5

- Discussion Questions
- Problems 1 & 3

Learning Objectives for Chapter 11

- After studying this chapter you should be able to:
  * describe the types of audits and auditors
  * provide an overview of the audit process for financial statement audits
  * describe the effects of computerization on the accounting process
  * briefly describe the audit process for financial statement audits
  * describe the essence and issues concerning the impact of SAS No. 55 on computer auditing

Learning Objectives for Chapter 11

- After studying this chapter you should be able to:
  * describe various computer auditing techniques and how they could be applied in database environments
  * distinguish between auditing around, auditing with and auditing through the computer
  * explain the process of auditing a relational DBMS
  * describe the implications of information technology on computer auditing

Information Systems Auditing

- Types of Audits
  - External Audits
  - Internal Audits
    - Operation of Internal Controls
    - Management or Operational
  - Compliance Audits

Information Systems Auditing

- Audit Steps
  * Establish Audit Objectives
  * Perform Audit Procedures
  * Evaluate Audit Evidence
  * Develop an Audit Opinion
  * Communicate Audit Results

Information Systems Auditing

- Auditing is the subject of another course
- We focus in this class only on how auditing is affected by the implementation of computerized accounting information systems

Information Systems Auditing

- Effects of Computerization
  * Decreased processing visibility
  * Data only in computer-readable form
  * Loss of visible audit trail
  * Extreme consequence of program errors
  * Lack of common sense
  * Increase in value of average fraud losses

Information Systems Auditing

- Offsetting benefits
  * Improved prevention
  * Electronic audit trail
  * Computer-assisted audit techniques

Information Systems Auditing

- SAS 48
  - * The auditor must assess
    - the extent of computerization of accounting
    - the complexity of computer-based systems
    - the degree to which audit evidence is in computer-readable form only
  - * and identify
    - computer-based controls

Information Systems Auditing

- SAS 55 (as amended by SAS 78 & 94)
  * Internal Control Structure
  * AR = IR x CR x DR
    - AR: Audit Risk
    - IR: Inherent Risk
    - CR: Control Risk
    - DR: Detection Risk
  * AR (Set by audit firm) = IR x CR (↑) x DR(↓)
  * Document understanding of internal control structure
  * Assess control risk (and test controls)
  * Amend substantive procedures accordingly

Information Systems Auditing

- Sarbanes-Oxley Act 2002 s.404
  - Distinguish
    - Internal controls over transaction processing
    - Internal controls over financial reporting
  - For public companies, with respect to internal controls over financial reporting
    - Management must now review, document and test
    - Management must issue a report on their work
    - External auditor **must** test management's work
    - Auditor issues a separate report on internal controls over financial reporting
    - Any major weakness requires an adverse report on internal controls

Information Systems Auditing

- Auditing Standard 5
  - The auditor must perform additional audit procedures to ascertain whether there are material weaknesses in internal control
    - If there is a material weakness, an adverse opinion on internal controls will be issued
    - Otherwise, an unqualified opinion will be issued on internal controls.
  - The external auditor is also required to issue an opinion on management's philosophy regarding internal controls over financial reporting
  - Auditors must perform a walkthrough of the accounting systems in order to understand how accounting transactions flow through the system
    - How the computer-based accounting system processes accounting transactions, from initiation of the transaction to eventual reporting in the financial statements
  - Automated controls are associated with lower risk than non-automated (manual) controls
  - Automated controls work consistently from year to year, assuming that the control itself has not changed and that general controls over program changes are effective and tested periodically.
  - The auditor's testing of information technology controls might focus on the application controls built into the pre-packaged software that management relies on to achieve its control objectives and the IT general controls that are important to the effective operation of those application controls

Information Systems Auditing

- Audit approaches and Computer Audit
  * Auditing around the computer
  * Auditing through the computer
    - Test data
    - Integrated Test Facility (ITF)
    - Embedded Audit Module
    - Mapping
    - Source code comparison
    - Parallel simulation
    - Reprocessing
  * Auditing with the computer

Information Systems Auditing

- Auditing with the computer
  * Utility programs
  * DQL (e.g., QBE in ACCESS)
  * Generalized Audit Software (e.g., IDEA, ACL)
    - Data retrieval
    - Calculations
    - Edit checks
    - Reformatting
    - File operations
    - Statistical sampling
    - Reports – "exception reports"

Information Systems Auditing

- Advanced Technology Environments
  - Concurrent auditing
    - Continuous auditing
  - Expert systems
  - Audit program generators
  - Audit workpapers
  - PC-based reference software

Group Work for Chapter 11

- Discussion Questions
- Problems 6 & 7

Hardware Performance

- Chapter 3 addresses Hardware and Software Technology
- A key idea discussed there is the *internal bus* or *system bus*
- This is a communication channel, or data path, that connects the CPU and the memory unit
- The Central Processing UNIT (CPU) has three main parts
  - Arithmetic-logic unit (ALU) – does the actual computation
  - Control unit (synchronized to the internal clock)
  - Registers
    - A *register* is a high-speed memory location inside the CPU

Hardware Performance

- The system bus has three main parts
  - Data bus – transmits data
  - Address bus – transmits addresses of memory locations
  - Control bus – transmits control signals (e.g., read, write, etc.)
- Each memory location is identified by its *address*
- Addresses are numbers: 0, 1, 2, 3, etc.
- Each bus is characterized by its *width*
- Think of this as the number of parallel wires in the path
- This is the number of separate bits that can be transmitted at once

Hardware Performance

- The original IBM PC had an 8088 processor that had a 20 bit address bus and an 8 bit data bus
- Thus, the data bus could transmit 8 bits simultaneously
- i.e., 1 byte of data could be moved from RAM to the CPU or from the CPU to RAM in a single move
- i.e., to move a standard 32 bit floating point (real) number (e.g., 3.14159) would take 4 moves of 8 bits!
- Typically, registers are designed to store as much data as can be transmitted on the data bus at one time
- Originally, the 8086 chip was designed with a 16 bit data bus and 16 bit registers – but the 8088, a "reduced" version of the 8086 used for the IBM PC, had only an 8 bit data bus

Hardware Performance

- The original IBM PC had an 8088 processor that had a 20 bit address bus and an 8 bit data bus
- Thus, the address bus could transmit 20 bits simultaneously
- i.e., addresses up to 2^{20} = 1,048,576 could be used
- i.e., up to 1MB of RAM could be addressed!
- (Due to a limitation in the Microsoft operating system, DOS, only 640 KB could actually be used)
- Memory is limited by:
  - The number of available addresses, based on the address bus
  - The number of memory locations on the memory chips fitted
    - IBM PC had from 16KB to 256KB

Hardware Performance

- Every CPU has a set of instructions that its ALU is able to interpret and execute
- Typically, the CPU can operate on numbers the size of its registers (the "word" size)
- Thus, the 8088 could directly add two 16 bit numbers
- In general, instructions sets have become larger and added new, more complex, instructions
  - For example, the 8088 included a Multiply instruction, so that the 8088 could directly multiply two 16 bit numbers
    - Prior CPUs, such as the Z80, could only do this by repeated addition
  - More complex instructions themselves may be longer
  - More complex instructions may take longer (i.e., more clock cycles) to execute

Hardware Performance

- Fetch-execute cycle
  - The CPU, systems bus, and RAM cooperate as follows
    - One register (PC) is used to store the address of the next instruction to be executed
    - That address is placed on the address bus
    - A 'read' signal is placed on the control bus
    - The instruction at that address in memory is transferred to the CPU
      - The data (instruction) is placed on the data bus
      - The data is transferred to the CPU
      - If the instruction is larger than the width of the address bus, this may take multiple moves
    - The instruction is interpreted and the address of the first data item it references is placed on the address bus
    - A 'read' signal is placed on the control bus
    - The data at that address in memory is transferred to a register in the CPU via the data bus
    - The address of the second data item referenced in the instruction is placed on the address bus
    - A 'read' signal is placed on the control bus
    - The data at that address in memory is transferred to a register in the CPU via the data bus
    - The CPU executes the instruction and retains the result in a register
    - The address in RAM where the result is to be stored is placed on the address bus
    - A 'write' signal is placed on the control bus
    - The data is transferred to the address in memory via the data bus
    - The PC register is updated to point to the next instruction to be executed

Hardware Performance

- A contemporary Pentium 4 is much more powerful than the original IBM PC
  * More complex instruction set
    - But average instruction takes more CPU cycles
  * 32 bit registers
  * 32 bit data bus can move 4 bytes at once
    - Took 4 cycles on 8088
  * 32 bit address bus allows up to 2^{32} memory locations = 4,294,967,296 = 4GB
    - Of course, you may not have bought that much RAM!
  * Finally, much faster clock speed (3.8 GHz v. 4.77MHz)

Hardware Performance

- Thus, performance and throughput of a PC are determined not just by processor speed, but by:
  - Complexity of instruction set
  - Average time (cycles) for instructions
  - Register size
  - Data bus width
  - Address bus width
  - Bus speed
  - Memory installed
  - Dual processors
  - Ram 'speed' – latency – e.g., time to store data in location once it is reached
  - Then there is the actual software itself, speeds of external devices, etc.

Sheldon Shirts

- Stage 7 – December 10
  - Produce Final Report on the project as described in the original assignment note
  - Remove Stage 6 printed materials only – leaving Stages 1–4, 7
  - For Stage 7, print & file Final Report as above, together with revised versions of:
    - Sales Revenue
    - Accounts Receivable (12/31/2006 & 3/31/2007)
    - Credit balances (12/31/2006 & 3/31/2007)
    - Aged Debts 3/31/2007
    - Prior Revenue written off by credits
    - Total Cash Receipts
    - Back Orders by Customer
    - Sales Analyses
      - Month
      - Product
      - Type of customer (D, M, X)
    - Returns Report
      - Show, by month & overall, total value shipped, value and % of resulting returns, value and % of credit notes issued
  - Combine databases, including tables, forms, queries, macros and reports, for all cycles & print the allocated report for each of the cycles
  - Submit databases via Digital Dropbox using previous naming conventions

Group Evaluation Forms

- Group Project Evaluation forms are due in class December 10 and are MANDATORY
- You cannot get credit for the Group Project without completing and submitting this form!
- Evaluations will be held confidential
- You will find that peer evaluations are a feature of professional life – treat them with seriousness, honesty and respect

Finally . . .

- Classes on Wednesday December 10 will be held in Levin Lab 005
- Please download, print, and bring to class the document "SAP R/3 Information Session" you will find on Blackboard at Course Documents: Resources